❖ SHIFT REGISTER

❖ Introduction

- Shift register is a sequential logic circuit whose output is depends on present input as well as past output.
- Shift register consists of group of same type of flip-flop.
- Shift register is used to store group of binary data and also used to shift the binary data.
- The total number of flip-flop present in shift register are depends on the total number of binary bits stored in shift register.
- If we have to store two bit binary data i.e 00,01,10,11 then shift register require two flip-flops.
- If we have to store three bit binary data i.e 000,001,010,011 upto 111 then shift register require three flip-flops.
- If we have to store four bit binary data i.e 0000, 0001, 0010, 0011 upto 1111 then shift register require four flip-flops.
- Then according to the logic, if we have to store 'N' bit binary data then shift register require 'N' no of flip-flops.

❖ Functions of Shift Register

- Shift register is used to store group of binary data and also used to shift the binary data.

  Or

- Data Storage and Data Movement.

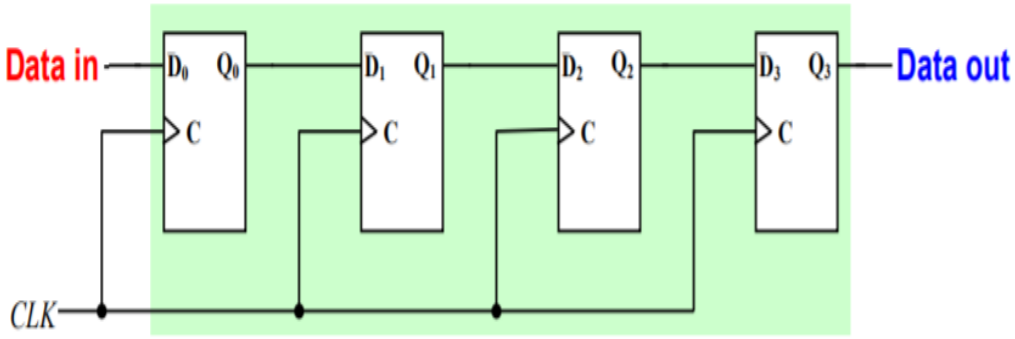
❖ Modes of Shift Register

- Left shift mode
- Right shift mode

❖ Types of Shift Register

1. Serial Input and Serial Output
2. Serial Input and Parallel Output
3. Parallel Input and Serial Output
4. Parallel Input and Parallel Output

❖ Serial Input and Serial Output Shift Register Block Diagram



Construction

- Figure shows the block diagram of Serial Input and Serial Output Shift Register which has D0,D1,D2,D3 are the Data inputs and Q0,Q1,Q2,Q3 are the Data output.
- Here we are applying single clock pulse to all the flip-flops to make all flip-flops simultaneously ON and OFF.
- This Shift Register is used to store 4 bit binary data i.e from 0000 to 1111 because it uses 4 flip flops.

- In this we are shifting binary data from **Right side to the left side.**

Truth Table:

Clock Pulse	Data Input	Q0	Q1	Q2	Q3	Data Output
↑		0	0	0	0	
↑	1	1	0	0	0	
↑	1	1	1	0	0	
↑	0	0	1	1	0	
↑	1	1	0	1	1	1
↑		0	1	0	1	1
↑		0	0	1	0	0
↑		0	0	0	1	1

Refer reference books for remaining types of shift register.

Counter

- Counter is a sequential logic circuit whose output is depends on present input as well as past output. Counter is a series connection of flips-flops or it is a group of flip-flops.
- The counter is used to count the total no states. The total no of states counted by the counter is depends on the no of bits stored in particular type of counter.
- If we are using two flip-flops in counter then two bit binary data i.e. 00,01,10,11 is stored in counter and total states counted by the counter are 4 and that are state0, state1, state2, state3.
- If we are using three flip-flops in counter then three bit binary data i.e. 000,001,010,011 upto 111 is stored in counter and total states counted by the counter are 8 and that are state0, state1, state2, state3 upto state7.
- If we are using four flip-flops in counter then four bit binary data i.e. 0000,0001,0010,0011 upto 1111 is stored in counter and total states counted by the counter are 16 and that are state0, state1, state2, state3 upto state15.
- If we are using N flip-flops in counter then N bit binary is stored in counter and total states counted by the counter are 2^N and that are state0, state1, state2, state3 upto stateN.
- The total states counted by the counter is calculated by 2^N formulae in which N is the value of total no. of bits stored in counter.

❖ Function of Counter

- To store the group of Binary Data and to Count the stored group of binary data.

❖ Types of Counter

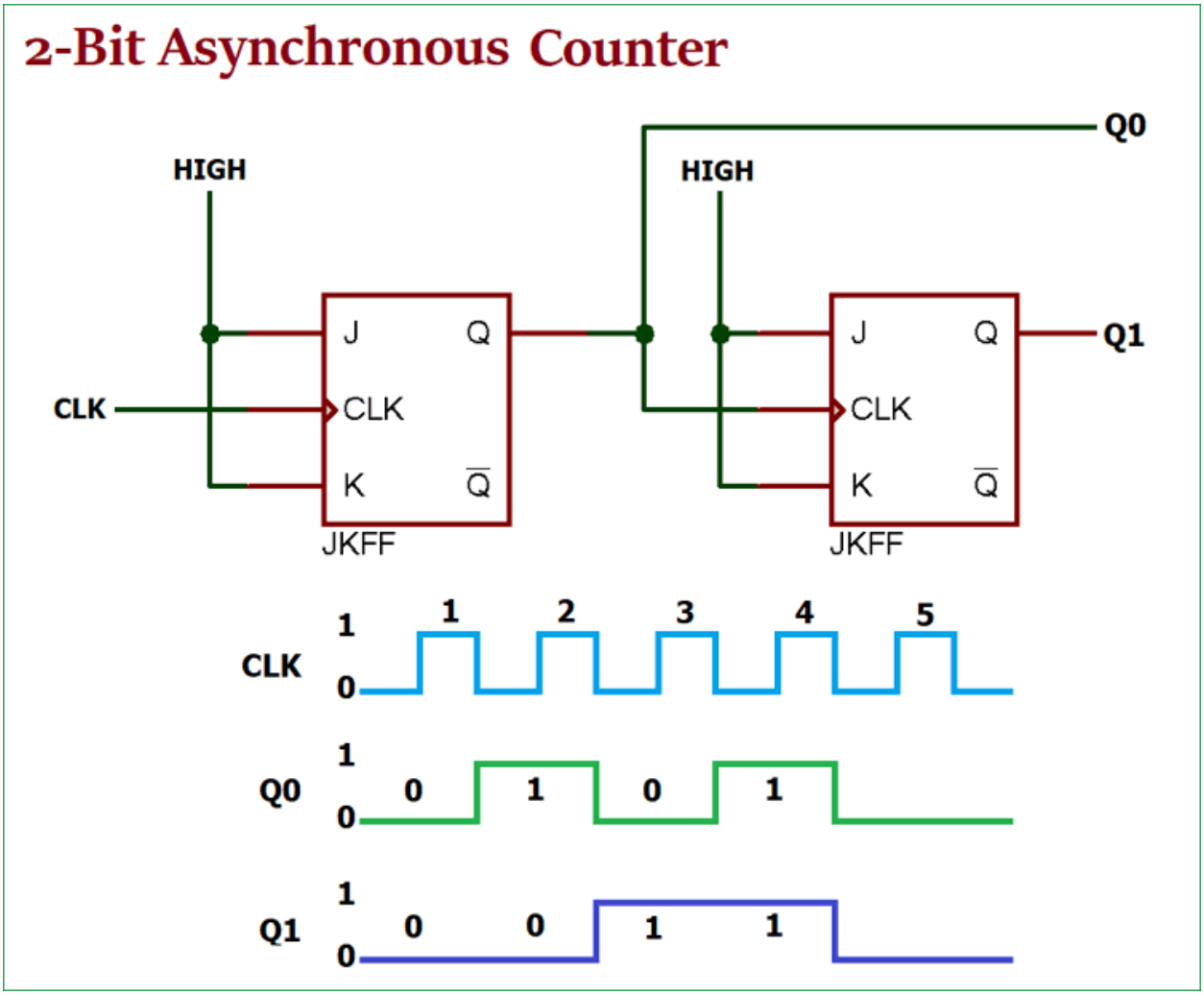
The types of counter is mainly depends of two factors the way in which clock signal is applied and the way in which counting is performed.

- Depending on the way in which clock signal is applied the Counter has two types:
  1. Synchronous Counter
  2. Asynchronous Counter
- Depending on the way in which counting is performed the Counter has two types:
  1. Up Counter
  2. Down Counter

1. **Synchronous Counter:** When same clock signal is applied to make simultaneously on or off all flip-flops are called as synchronous counter.
2. **Asynchronous Counter:** When every flip-flop has separate clock signal i.e first flip-flop has clock signal and for remaining flip-flop output of previous flip flop act as a clock signal for next flip-flop this connection is called as asynchronous counter.

3. **Up Counter:** When the flip-flop is performing counting in ascending order i.e from 0 to n then the flip is called as Up Counter.
4. **Down Counter:** When the flip-flop is performing counting in descending order i.e from n to 0 then the flip is called as down Counter.

1. 2 bit Asynchronous Up Counter



Truth Table

Clock Signal	Q0	Q1	State
↑	0	0	State0
↑	0	1	State1
↑	1	0	State2
↑	1	1	State3

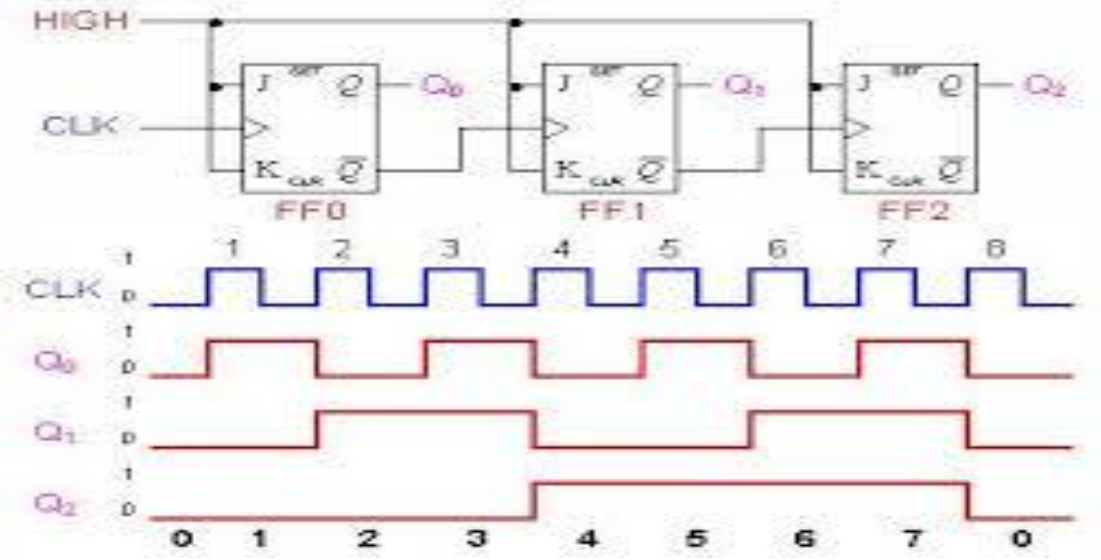
Figure shows the block diagram of two bit Asynchronous Up Counter which has J,K are the applied inputs and Q,Q^- are the output.

This counter uses two JK flip-flops because it is a 2 bit counter which stores 2 bit group of binary data i.e. 00,01,10,11 and the total no states counted by the counter are 4 by applying 2^n formulae in which n is the value of no of bits stores in flip-flop.

This is a asynchronous type of counter in which separate clock signal is applied to first flip-flop and for remaining flip-flop the output of previous flip-flop is applied as a clock signal to next flip-flop.

This is a Up type of counting which considers output of upward directions such as Q1,Q2. this counter performs counting in ascending order i.e. from 0 to n. this counter stores 2 bit binary data and it has 4 states from state0 to state3.

2. 3-Bit Asynchronous Down Counter



Truth Table

Clock Signal	Q2	Q1	Q0	State
↑	1	1	1	State7
↑	1	1	0	State6
↑	1	0	1	State5
↑	1	0	0	State4
↑	0	1	1	State3
↑	0	1	0	State2
↑	0	0	1	State1
↑	0	0	0	State0

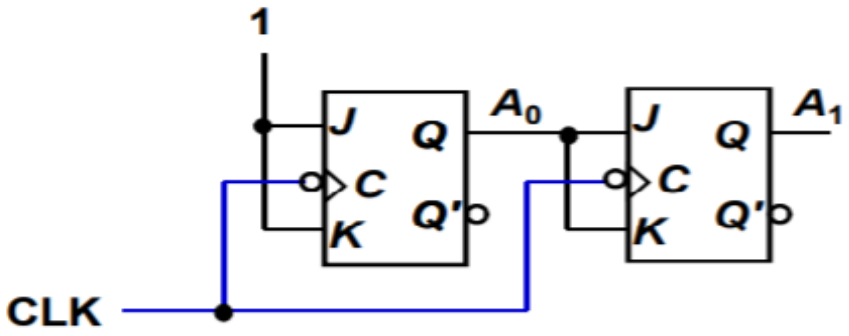
Figure shows the block diagram of three bit Asynchronous down Counter which has J,K are the applied inputs and Q,Q^{-} are the output.

This counter uses two JK flip-flops because it is a 3 bit counter which stores 3 bit group of binary data i.e. 000,001,010,011 upto 111 and the total no states counted by the counter are 8 by applying 2^n formulae in which n is the value of no of bits stores in flip-flop.

This is a asynchronous type of counter in which separate clock signal is applied to first flip-flop and for remaining flip-flop the output of previous flip-flop is applied as a clock signal to next flip-flop.

This is a down type of counting which considers output of downward directions such as $Q1^-$,$Q2^-$,$Q3^-$. this counter performs counting in descending order i.e. from n to 0. this counter stores 3 bit binary data and it has 8 states from state7 to state0.

3.Two bit Synchronous Up Counter



Truth Table

Clock Signal	Q0	Q1	State
↑	0	0	State0
↑	0	1	State1
↑	1	0	State2
↑	1	1	State3

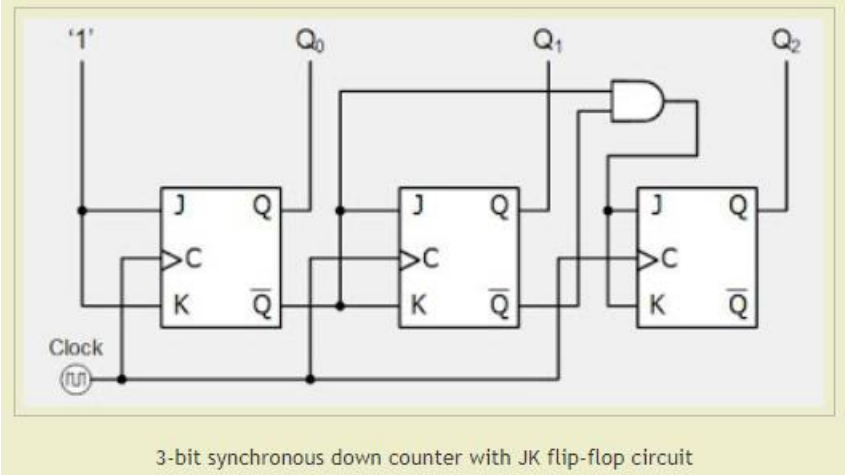
Figure shows the block diagram of two bit Synchronous Up Counter which has J,K are the applied inputs and Q,Q^- are the output.

This counter uses two JK flip-flops because it is a 2 bit counter which stores 2 bit group of binary data i.e. 00,01,10,11 and the total no states counted by the counter are 4 by applying 2^n formulae in which n is the value of no of bits stores in flip-flop.

This is a Synchronous type of counter in which single clock signal is applied to all flip-flop which are present in particular type of counter.

This is a Up type of counting which considers output of upward directions such as Q1,Q2. this counter performs counting in ascending order i.e. from 0 to n. this counter stores 2 bit binary data and it has 4 states from state0 to state3.

4.3-Bit Synchronous Down Counter



3-bit synchronous down counter with JK flip-flop circuit

Truth Table

Clock Signal	Q2	Q1	Q0	State
↑	1	1	1	State7
↑	1	1	0	State6
↑	1	0	1	State5
↑	1	0	0	State4
↑	0	1	1	State3
↑	0	1	0	State2
↑	0	0	1	State1
↑	0	0	0	State0

Figure shows the block diagram of three bit Synchronous down Counter which has J,K are the applied inputs and Q,Q^- are the output.

This counter uses two JK flip-flops because it is a 3 bit counter which stores 3 bit group of binary data i.e. 000,001,010,011 upto 111 and the total no states counted by the counter are 8 by

applying 2^n formulae in which n is the value of no of bits stores in flip-flop.

This is a Synchronous type of counter in which single clock signal is applied all flip-flop which are present in particular type of counter.

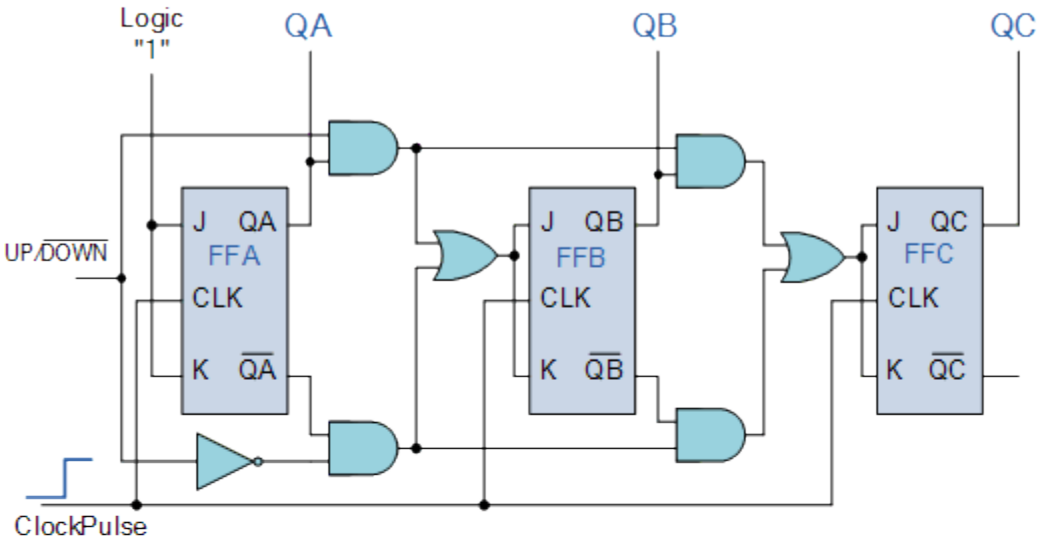
This is a down type of counting which considers output of downward directions such as $Q1^-$,$Q2^-$,$Q3^-$. this counter performs counting in descending order i.e. from n to 0. this counter stores 3 bit binary data and it has 8 states from state7 to state0.

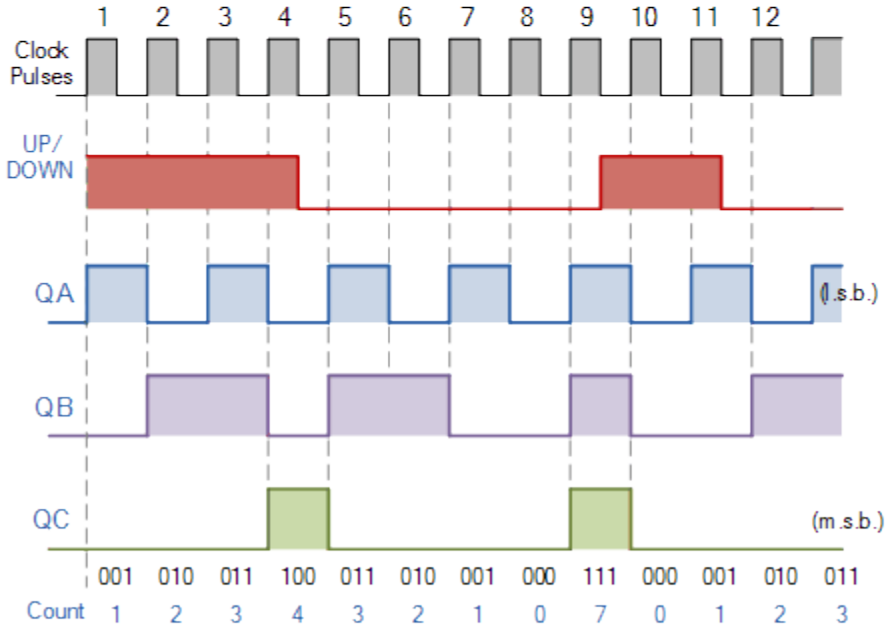
3 Bit Synchronous Up- Down Counter

The circuit above is of a simple 3-bit Up/Down synchronous counter using JK flip-flops configured to operate as toggle or T-type flip-flops giving a maximum count of zero (000) to seven (111) and back to zero again. Then the 3-Bit counter advances upward in sequence (0,1,2,3,4,5,6,7) or downwards in reverse sequence (7,6,5,4,3,2,1,0).

Generally most bidirectional counter chips can be made to change their count direction either up or down at any point within their counting sequence. This is achieved by using an additional input pin which determines the direction of the count, either Up or Down and the timing diagram gives an example of the counters operation as this Up/Down input changes state.

Nowadays, both up and down counters are incorporated into single IC that is fully programmable to count in both an “Up” and a “Down” direction.





Difference Between Synchronous and Asynchronous Counter

Sr.No	Parameter	Synchronous Counter	Asynchronous Counter
1	Components Required	High	Less

2	Requirements of Gates	Extra logic gates are required	No extra logic gates are required
3	Operating Frequency	Operating Frequency is high	Operating Frequency is low
4	Speed	Slower	Faster
5	Cost	High	Low
6	Design Complexity	Easy to design	Difficult to design
7	Clock Signal	Clock is same to all flip-flops.	Clock signal is different to all flip-flops.