Digital counters

B Sc III Electronics

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Digital counters

Introduction

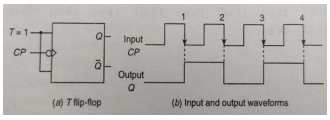
- Digital counter is a sequential circuit that counts the occurrence of clock pulses applied to it.it also called as frequency divider.
- There are many kinds and designs of these counters but almost all of them are built by connecting flip-flops as the basic units.
- When the clock pulses to be counted are applied to the input of a counter, the flip-flops in it go through a sequence of states, one after the other, which are decoded to read the counts.
- On reaching the highest count, the counter completes its counting cycle and returns back to its initial (reset) state. Digital counters designed to count either in an upward sequence (from lower toward higher counts), or in the downward sequence (from higher toward lower counts).
- They can also be built to start counting from any desired count other than 'zero'.
- Most of the counters follow the natural-binary sequence of counting, while some others may follow some other sequence.

Broadly, the digital counters can be divided into the following two categories.

1. Asynchronous (or ripple) counters:- In asynchronous counters all the flip-flops are not clocked simultaneously, i.e. they do not trigger at the same time.
2. Synchronous (or parallel) counters:- In synchronous counters, all the flip-flops are clocked simultaneously, i.e. all of them trigger at the same time in synchronism with a clock.

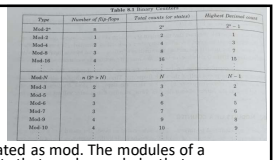
Before we go into detailed discussion of various types of counter-circuits, let us first see how a single flip-flop operates as a basic counter.

Basic flip flop counter



- Fig. shows a negative edge-triggered T flip-flop which is obtained from a JK flip-flop by Joining the J and K inputs together into a single input T.
- When we keep T= 1,and apply clock pulses to the CP input of this flip-flop, it toggles (changes state) at every negative clock-edge.
- The normal output Q, along with the clock-input CP, are shown in the waveform diagram of Fig. It can be noted in this diagram that the output Q goes high at the first negative edge and then at the third negative edge, i.e. after every two clock-pulses.
- Similarly, it goes low after every two clock-pulses. It means that the numbers of pulses counted by this flip-flop is twice the number of times Q goes low (or high), and hence it functions as a counter.

MODULES OF A COUNTER



- Counters are identified by their modulus abbreviated as mod. The modules of a counter is expressed by the total number of counts that can be made by that counter, or the total number of state through which the counter goes in one complete counting-cycle before it resets back to its initial state.
- Thus, a binary counter using n flip-flops has 2 total counts (or states),and so it has Modulus = 2 and the name as mod 2" counter.
- Specifically, a mod-2 counter uses a single flip-flop and counts 2 pulses, a mod-4 counter uses two flip-flops and counts 4 pulses, a mod-8 counter uses three flip-flops and counts 8 pulses, and so on.
- These counters are also called as divide-by-2" counters because they divide the clock frequency by 2". Usually, the natural binary counting-sequence is followed in these counters. eeApart from the above, there is another group of counters whose modulus N is not equal to 2(N2") Designated as mod-N, these counters include mod-3, mod-5 mod-6, mod-7, mod-9through mod-15, and so on, which can be built from mod-2" counters by eliminating the unwanted extra counts.

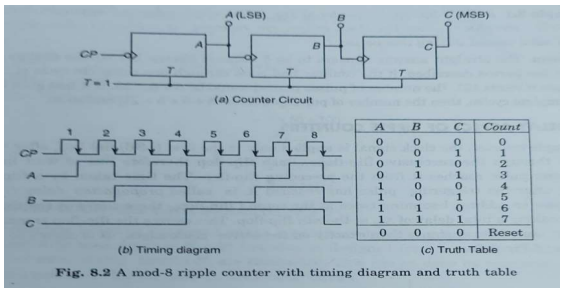
Asynchronous counters

- Asynchronous counters are not synchronized with the clock. The flip-flops in these counters are cascaded in **series**, such that the output of one is connected to the input of the other.
- Since the clock is connected only to the input of the first flip-flop, each flip-flop triggers when the pulse-signal reaches it (like a ripple) after passing through the preceding flip-flops one after the other, and hence the name "ripple" counter.
- Since each flip-flop takes some time (called propagation delay) to trigger (to change state) after the triggering pulse reaches it, the last flip-flop triggers after a cumulative delay of all the flip-flops. This aspect makes the asynchronous counters to suffer from slower speed of operation compared with the synchronous counters.

MOD-8 RIPPLE COUNTER

- mod-8 ripple counter is an asynchronous counter that counts 8 pulses.
- It uses 3 flip-flops (because 2n = 8 gives n =3). Fig. shows this circuit with 3 flip-flops (A, B, C), say of T type, in cascade, such that the output of each flip-flop is connected to the CP input of the next, and the clock is connected to the CP input of the first (A).
- When the T input of each flip-flop is kept high (T = 1), each one toggles to the opposite state when negative clock-edge strikes it. Because the LSB flip-flop A receives each CP, it toggles at each negative edge, while B and C toggle less often because they receive the negative edges from the preceding flip-flops.
- For example, when A toggles from 1 to 0, B receives negative edge and toggles. Like wise, when B goes from 1 to 0, C gets a negative edge and toggles.
- In this way, a flip-flop toggles whenever its preceding flip-flop resets to 0, as shown in the timing diagram.

Mod 8 ripple counter



A	B	C	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	Reset

Fig. 8.2 A mod-8 ripple counter with timing diagram and truth table

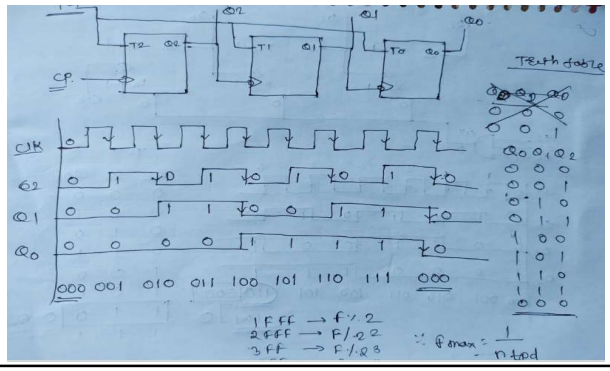
- Keeping this behavior in mind, and using the truth table Fig. the operation of this counter is explained as below.
- Operation

1. Initially Before applying the clock pulses, let all the flip-flops be in the 0 state so that the number stored in the counter is CBA = 000.

2. At the end (negative-edge) of CP 1:A goes from 0 to 1, but the flip-flops B and C do not, because there is no negative edge present at their CP inputs. Thus, the count becomes CBA = 001.

3. At the end of CP 2 : A goes from 1 to 0. This creates the negative edge to flip-flop B, therefore B goes from 0 to 1. Flip-flop C does not change state for the reason stated above. Thus, the count is CBA = 010.At the end of CP3: A goes from 0 to 1, with no triggering of B or C. This gives, CBA4.= 011.5.Counting in this way we would next get the counts CBA = 100, 101, 110 and 111 at the ends of pulses 4, 5, 6 and 7, respectively.6. Finally, at the end of CP 8 : All the flip-flops return back to the 0 (reset) state giving CBA =000.

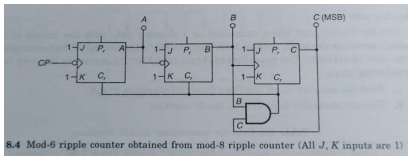
- Frequency division As indicated in the timing diagram of Fig. 3.2(6) the frequency of transitions of flip-flop A is one-half, that of B is one-fourth, and that of C is one-eighth of the clock frequency, and therefore this counter is also termed as a divide-by-8 counter.



MOD-6 RIPPLE COUNTER

- A mod-6 ripple counter has six states (000, 001, 010, 011, 100 and 101). This counter can be obtained by modifying a basic mod-8 counter using the foregoing procedure of clearing AND/NAND gate. Its circuit using the JK flip-flops (A, B, C) with preset and clear (P, C,)asynchronous inputs, is shown in Fig. 8-4. The AND gate is used to eliminate the two extra states (110 and (111) of the basic counter.

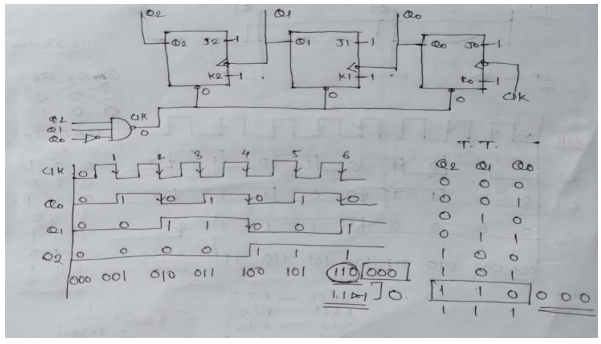
Fig.



8.4 Mod-6 ripple counter obtained from mod-8 ripple counter (All J, K inputs are 1)

Operation :-

Initially, let all the flip-flops be in the reset states, reading the count as CBA = 000. When CPs are applied, the counting advances in the natural sequence from 001 at the first CP, 010at the second, and so on, upto 101 at the fifth CP. The AND gate, because of remaining disabled, does not affect this counting operation. However, when the count reaches 110 at the sixth CP, the AND gate is enabled (because B and C both go high) and therefore it clears all the flip-flops to the reset state of CBA = 000. The two unwanted states 110 and 111 are skipped off in this manner.



ASYNCHRONOUS MOD-8 DOWN Counter

- ASYNCHRONOUS MOD-8 DOWN counter down counter is one that counts in the downward sequence i.e. from a higher count toward the lower counts. Such a counter can be built from a normal (up) counter, if we connect the inverted output (instead of normal output) from each flip-flop to the CP input of the next. Fig. 8-5 (a) shows an asynchronous mod-8 down counter using three JK flip-flops (A,B, C). Clock pulses are supplied to the CP input of the first flip-flop A, while the inverted outputs A and B are connected to the CP inputs of flip-flops B and C, respectively

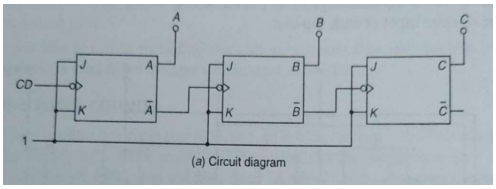
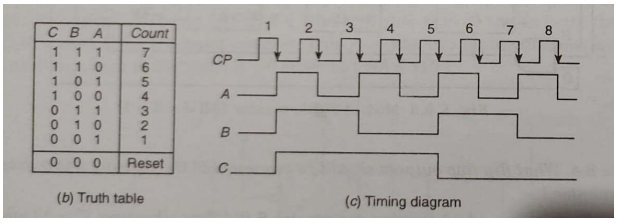
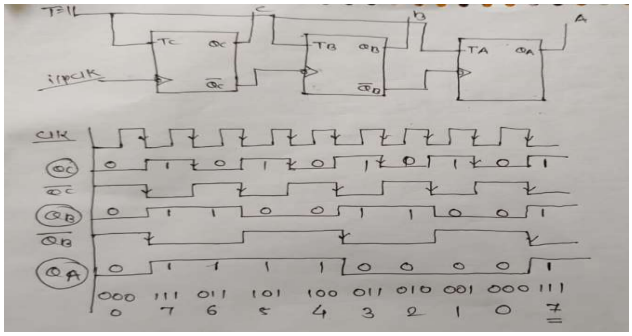


Fig (a) shows an asynchronous mod-8 down counter using three JK flip-flops (A,B, C). Clock pulses are supplied to the CP input of the first flip-flop A, while the inverted outputs A and B are connected to the CP inputs of flip-flops B and C, respectively.

In a normal asynchronous counter, "the first flip-flop toggles at each CP, and the others toggle whenever the preceding flip-flop goes from 1 to 0 state". However in a down counter, he later statement must be reversed, i.e. "each flip-flop toggles when its preceding flip-flop goes from 0 to 1 state." Thus the flip-flop A toggles at each clock edge, B toggles when A goes from 0 to 1, and C toggles when B goes from 0 to 1.

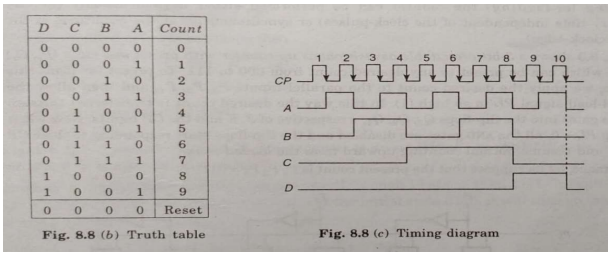
In this way, this counter passes through 8 states starting from the highest count 111 (7) at the first clock-edge, and ending with the lowest count 001 at the seventh edge. The counter then resets to 000 at the eighth clock-edge. These transitions are given in the truth table of Fig. 8.5 (b), as also shown in the timing diagram of Fig. 8.5 (c).



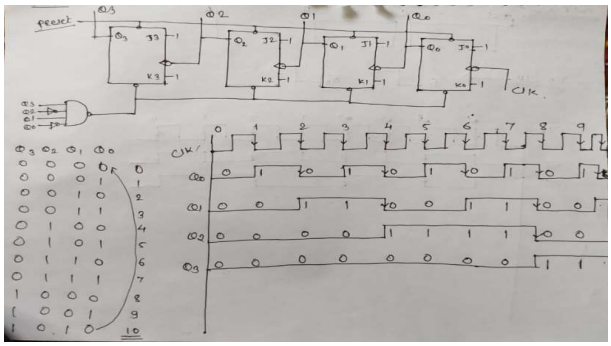


Asynchronous MOD-10 (DECADE) Counter :-

- A mod-10 (or decade) counter has ten distinct states which can progress in any desired kind of sequence. However, when a decade counter progresses only in natural-binary sequence, it is then termed as BCD counter.
- An asynchronous BCD counter using four negative-edge-triggered JK flip-flops (A, B, C, D) in cascade, is shown in Fig. (a) along with its truth table in (b) and timing diagram in (c).Note that the unconnected inputs (J inputs of flip-flops A and C, and K inputs of all the flip-flops) are held at 1 level.
- Normally, 4 flip-flops can go to count up to 16 pulses. However, the present circuit is made to count up to 10 pulses (discarding the extra 6 states) with highest count as DCBA = 1001, after which it resets as follows.



The inputs to the AND gate are the outputs from the flip-flops B and C, which are both at 0before the 10th pulse. With the 0 output from the AND gate applied to J input of flip-flop D, it triggers from 1 to 0. The flip-flop A also triggers from 1 to 0 at this time. Thus, all the flip-flops are reset to count DCBA = 0000 at the end of 10th pulse. This is also illustrated in the timing diagram of Fig, 8.8 (c).



DISADVANTAGES OF ASYNCHRONOUS COUNTERS :-

The asynchronous/ ripple counters suffer from the following main disadvantages:

- They operate with lower speeds because of the accumulated propagation-delay.
- They generate narrow spikes at the decoder-outputs.
- They cannot operate at very high clock-frequencies, especially when the number of bits is large.

Despite the above disadvantages, asynchronous counters are still preferred in many applications because of their simpler circuitry.

SYNCHRONOUS COUNTERS :-

- In a synchronous counter, all the flip-flops are triggered simultaneously by the pulses from a common clock.
- In this way, the propagation delay is considerably reduced to the delay of only one flip-flop plus the delay time of the control gates.
- This raises the operating speed of the counter and allows higher clock-frequencies to be used. The maximum clock frequency for a synchronous counter is typically (30 MHz) about twice that (18 MHz) for a ripple counter.
- Also the power dissipation is reduced to one-half of the latter case. Since no spikes appear in the output, no strobe signal is required in the decoding of these counters.
- However, the designing of synchronous counters is much more difficult than a ripple counter, because it involves a cumbersome synthesis procedure using Karnaugh maps.

Synchronous counters are of two types depending on using a serial carry or a parallel carry.

Synchronous MOD-16 Counter (Serial Carry):-

- One arrangement for a mod-16 (4-bit) synchronous counter with serial carry is shown in Fig.(a) using four negative-edge-triggered T flip-flops (A, B, C, D), all clocked simultaneously with a common clock (CP).
- The two AND gates (A1 and A2) are required as control gates. It can be noted in this circuit that only the T1 input of the LSB flip-flop is held at 1 level, while for the other flip-flops their T inputs are obtained as some combinations of flip-flop outputs as determined below.

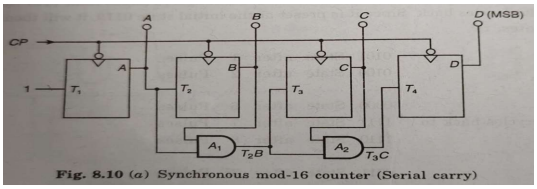


Fig. 8.10 (*a*) Synchronous mod-16 counter (Serial carry)

D	*C*	*B*	*A*	*Count*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15
0	0	0	0	Reset

Fig. 8.10 (*b*) Truth table for Fig. 8.10 (*a*)

Determination of inputs T1, T2, T3, T4 From the truth table of Fig. (b), we observe and logically deduce as follows.

1. Flip-flop A toggles at each pulse, for which we must have
   T1=1
2. Flip-flop B toggle when A = 1, therefore we must have
   T2 = A.
3. Flip-flop C toggles when both A =B = 1, therefore we must have
   T3 = AB =T2B
4. Flip-flop D toggles when A = B = C= 1, which leads to have
   T=ABC = T3C

A2, 1 and p-flop inpu t the trig er the othe Max -flops Min

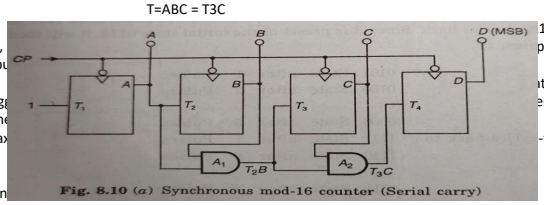


Fig. 8.10 (*a*) Synchronous mod-16 counter (Serial carry)

SYNCHRONOUS MOD-10 (DECADE) COUNTER (Parallel Carry)

A synchronous mod-10 decade counter with parallel carry can be formed from the mod-16 counter of Fig. with a little modification by using an additional AND gate A, as shown in Fig. (a), so as to eliminate the six unwanted states after the tenth state.

In this circuit, we use four JK flip-flops, which are negative-edge-triggered and synchronously clocked. The counting sequence goes upto DCBA = 1001 as indicated in the truth table of Fig. (b), after which the counter resets to DCBA = 0000, instead of going to the 11th state.

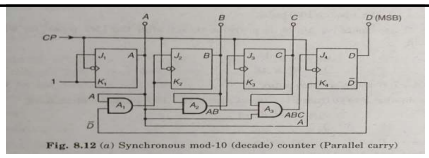


Fig. 8.12 (*a*) Synchronous mod-10 (decade) counter (Parallel carry)

D	C	B	A	Count
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
0	0	0	0	Reset

Fig. 8.12 (*b*) Truth table of mod-10 counter

Determining J-K Inputs

- To deduce the logic for J-K inputs, let us consider the states of the flip-flops before and after the 10th pulse in the truth tables of mod-16 and mod-10 counters, which are rewritten as follows

	Mod-16 DCBA	Mod-10 DCBA
Before the 10th pulse :	1001	1001
After the 10th pulse :	1010	0000

We observe that

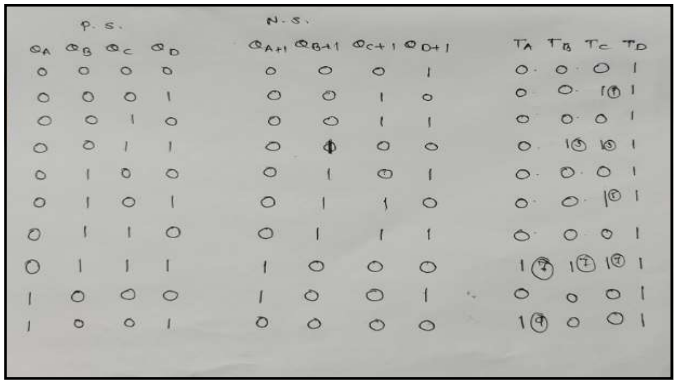
1. Flip-flop A toggles to 0 after 10th pulse, therefore we must have
   J1= K1= 1

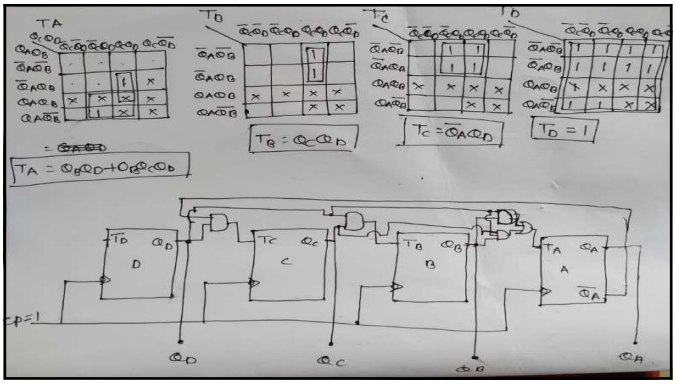
2. Flip-flop B toggles when A =1. But B has to remain in its previous state 0 after 10thpulse, therefore to keep B inactive, we must have
   J2= K2=0
   Or J2= K2 = AD .....(1)
   because A = 1,D= 1 before 10th pulse.

3. Flip-flop C also has to remain in its previous state 0 after the 10th pulse, for which we must have
   J3= K3=0
   Or J3= K3 = AB .....(2)
   because A = 1, B = 0 before 10th pulse.

4. To allow flip-flop D to go from 1 to 0 (reset state) after 10th pulse we must have
   J4 =0 and K4=1
   Or J4= ABC and K4=A ..... (3)
   because A = 1, B =0, C=0 before 10th pulse.

Logic equations (1), (2) and (3) are implemented using the gates A1, A2 and A3, in fig (a).





APPLICATIONS OF COUNTERS

Counters are used in digital computers, data processing systems and industrial control systems for a variety of applications, some of which are:

1. Direct counting.
2. Dividing the frequency of a wave.
3. Measuring a frequency and time.
4. Measuring the distance or speed of an object.
5. Counting the sequence of operations in a Computer.

DIGITAL CLOCK :-

One of the most important applications of digital counters is a digital clock that displays the daily time in terms of hours, minutes and seconds.

The essential requirement in the construction of a digital clock is an accurately controlled basic clock-frequency, which can be obtained from a quartz-crystal oscillator, or from the ac-power line. Fig. shows the black diagram for a digital clock operated with a clock frequency of 50 Hz.

This arrangement has three sections "seconds" section, "minutes" section and "hours" section. In the "seconds" and "minutes" sections each, the frequency is divided by 60 using a BCD counter and a mod-6 counter. How this clock arrangement operates is explained below.

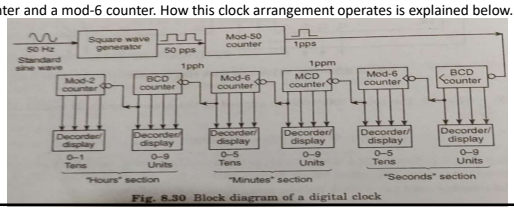


Fig. 8.30 Block diagram of a digital clock

First of all, the 50 Hz sine-wave signal obtained from a standard source is converted into square pulses at the rate of 50 pulses per second (pps) by a square wave generator.

This 50 PPS waveform goes through a mod-50 counter which divides the 50 pps to 1 pps. Now, the 1 PPS signal is sent into the "seconds" section, which counts and displays seconds from 0 through 59.

The BCD counter advances one count per second and recycles to 0. This triggers mod-6 counter and causes it to advance by one count. This continues for 59 seconds, at which the mod-6 counter is at 101 (5) count, and the BCD counter is at 1001 (9),which in turn recycles the mod-6 counter to 0.

The output of mod-6 counter of "seconds" section which has a frequency of 1 ppm, is fed into the "minutes" section, which counts and displays minutes from 0 through 59. This section operates similar to the "seconds" section.

The output of mod-6 counter of the "minutes" section which has a frequency of 1 pph, is fed to the "hours" section which counts and displays hours from 1 to 12. This section never goes to the zero-state like the "minutes" or "seconds" sections.